AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 5 line 22 and ending on page 6 line 8 with the following:

This invention features a fractional-N synthesizer with programmable output phase including a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal. The phase locked loop includes a frequency divider, a synchronization circuit responsive to the input reference signal for generating synchronization pulses at integer multiples of M periods of the input reference signal. An interpolator is responsive to F and M ~~an input fraction F/M~~, where F is the fractional value and M is the modulus, to provide to the frequency divider an output which is a fractional value equal to, on average, the input fraction F/M. A phase adjustment circuit responsive to the synchronization circuit for varies the phase of the output signal with respect to the input reference signal.

Please replace the paragraph beginning on page 6 line 18 and ending on page 7 line 6 with the following:

This invention also features a fractional-N synthesizer with programmable output phase including a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal. The phase locked loop includes a frequency divider, a synchronization circuit responsive to the input reference signal for generating synchronization pulses at integer multiples of M periods of the input reference signal, a phase register including a predetermined phase adjustment value, and an interpolator responsive to F and M ~~an input fraction F/M~~, where F is the fractional value, and M is the modulus, and a phase register. The interpolator provides to the frequency divider an output which is a fractional value equal to, on average, the input

fraction F/M. An enable signal applied to the synchronization circuit resets the interpolator with the predetermined phase adjustment value to vary the phase of the output signal with respect to the input reference signal.

Please replace the paragraph on page 8 beginning on line 4 and ending on line 16 with the following:

This invention also features a fractional-N synthesizer with programmable output phase including a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal. The phase locked loop includes a frequency divider, and a synchronization circuit responsive to the input reference signal for generating synchronization pulses at integer multiples of M periods of the input reference signal. An interpolator is responsive to F and M ~~an input fraction F/M~~, where F is the fractional value and M is the modulus, to provide to the frequency divider an output which is a fractional value equal to, on average, the input fraction F/M. A phase adjustment circuit responsive to the synchronization circuit for varies the phase of the output signal with respect to the input reference signal. The phase adjustment circuit includes a switching circuit for selectively applying the fractional value and a modified fractional value to the interpolator to define a predetermined phase relationship between the output signal and the input reference signal.